UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/801,812	02/14/1997	JOHN H. GIVENS	2269-6888US (95-1078.00/U	6774

24247 7590 02/26/2008

TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER	
MALDONADO, JULIO J	
ART UNIT	PAPER NUMBER
2823	

NOTIFICATION DATE	DELIVERY MODE
02/26/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTOMail@traskbritt.com

Office Action Summary	Application No.	Applicant(s)	
	08/801,812	GIVENS, JOHN H.	
	Examiner	Art Unit	
	JULIO J. MALDONADO	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9-15 and 64-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 9-15 and 64-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The addition of claims 65 and 66 as set forth in the reply filed on 01/17/2008 is acknowledged.

2. Claims 1-6, 9-15 and 64-66 are pending in the application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6, 9-14 and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeSilva (U.S. 5,926,736) in view of Fiordalice et al. (U.S. 5,420,072, hereinafter Fiordalice) and Huang et al. (U.S. 5,008,216, hereinafter Huang).

In reference to claims 1-5, 9-13 and 64, DeSilva (Figs.1-5) teaches a method of forming an interconnect structure including the steps of forming a recess (106, 112) within a dielectric material (102) situated on a substrate (100), the recess (106, 112) extending below a top surface of the dielectric material (102); forming a diffusion barrier layer (116) substantially conformally on the top surface of the dielectric material (102)

and over an interior surface of the recess (106, 112); forming an electrically conductive layer (118) on the barrier layer (116) over the top surface of the dielectric material (102) and substantially within the recess (106, 112) such that voids (120, 122) are present within the recess; forming an energy absorbing layer (124) on the electrically conductive layer (118), the energy absorbing layer (124); and utilizing a furnace to apply energy to the energy absorbing layer (124) sufficient to cause the electrically conductive layer (118) to fill the voids (120, 122) within the recess (120, 122) (DeSilva, column 2, line 30 – column 5, line 30).

Furthermore, DeSilva teaches wherein the barrier layer is made of titanium (DeSilva, column 2, lines 54 – 63), the conductive material is made of aluminum (Desilva, column 2, lines 66 – 67) and wherein the energy absorbing layer is made of titanium nitride (DeSilva, column 3, lines 5 – 10).

DeSilva fails to disclose wherein said substrate is a semiconductor substrate; forming a seed layer on the diffusion barrier layer over the top surface of the dielectric material and within the recess, the diffusion barrier layer comprising a material having a melting point greater than or equal to that of a material comprising the seed layer, wherein the material comprising the seed layer is made of aluminum, titanium nitride, titanium, titanium aluminide or comprises tungsten, wherein the seed layer and the barrier layer are formed by a chemical vapor deposition process; prior to forming a seed layer on the diffusion barrier layer, heating the diffusion barrier layer in an environment substantially containing a nitrogen gas; and removing portions of the energy absorbing

layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

However, Fiordalice (Figs.1-8) teaches a method to form an interconnect structure including the steps of forming a recess (16) within a dielectric material (14) situated on a semiconductor substrate (12), the recess extending below a top surface of the dielectric material (14); forming a diffusion barrier layer (24) on the top surface of the dielectric material (14) and over an interior surface of the recess (16), wherein said barrier layer (22) is made of titanium nitride by a chemical vapor deposition process; forming a seed layer (24) on the diffusion barrier layer (22) over the top surface of the dielectric material (14) and within the recess (16), wherein the material comprising the seed layer (24) is made of titanium nitride by a chemical vapor deposition process and wherein prior to forming a seed layer (24) on the diffusion barrier layer (22), heating the diffusion barrier layer in an environment substantially containing a nitrogen gas; forming an electrically conductive layer (26) made of aluminum on the seed layer (24) over the top surface of the dielectric material (14) and within the recess (16); and removing portions of the electrically conductive layer (26) that are situated above the top surface of the dielectric material (14) by a chemical mechanical polishing process (Fiordalice, column 2, line 21 – column 5, line 34).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of DeSilva and Fiordalice to enable providing a semiconductor substrate in DeSilva according to the teachings of Fiordalice because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or

useful methods of providing the disclosed substrate in DeSilva and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

It would also have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of DeSilva and Fiordalice to enable forming a barrier layer and a seed layer in DeSilva according to the teachings of Fiordalice because this would result in improved electromigration resistance (Fiordalice, column 1, lines 45 – 52) and improved deposition of further conductive layer over said seed layer (Fiordalice, column 4, lines 24 – 29).

Also, it would have been within the scope of one of ordinary skill in the art to combine the teachings of DeSilva and Fiordalice to enable removing overlying layers above the dielectric layer of DeSilva according to the teachings of Fiordalice because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of removing overlying layers above said dielectric layer in DeSilva and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combined teachings of DeSilva and Fiordalice fail to disclose wherein the seed layer is made of tungsten or a material different than that of the barrier layer.

However, Huang (Figs.1-8) teaches a method to form an interconnect structure including the steps of forming a recess (13) within a dielectric material (3, 11) situated on a semiconductor substrate (1), the recess (13) extending below a top surface of the dielectric material (3, 11); forming a diffusion barrier layer (9) on the top surface of the

dielectric material (3, 11) and over an interior surface of the recess (13), wherein said barrier layer (9) is made of titanium; forming a seed layer (21) on the diffusion barrier layer (9) over the top surface of the dielectric material (3, 11) and within the recess (13), wherein the material comprising the seed layer (21) is made of tungsten, tantalum, or any other refractory metal; forming an electrically conductive layer (17) made of on the seed layer (21) over the top surface of the dielectric material (3, 11) and within the recess (13); and removing portions of the electrically conductive layer (17) that are situated above the top surface of the dielectric material (3, 11) (Huang, column 4, line 42 – column 5, line 31).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of DeSilva, Fiordalice and Huang to enable forming the seed layer of the combination of DeSilva and Fiodalice according to the teachings of Huang because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods and materials for the disclosed seed layer of De Silva and Fiordalice and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claim 6, the combined teachings of DeSilva, Fiordalice and Huang teach depositing tungsten by a chemical vapor deposition process (Fiordalice, column 4, lines 51 - 66).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable forming the tungsten seed layer using the deposition

process in the combination of DeSilva, Fiordalice and Huang because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of forming the disclosed seed layer and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claim 14, the combined teachings of DeSilva, Fiordalice and Huang substantially teach all aspects of the invention but fail to expressly disclose wherein the recess has an aspect ratio greater than about four to one. However, one of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization to obtain a desired contact opening. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV)(B).

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over DeSilva ('736) in view of Fiordalice ('072) and Huang ('216) as applied to claims 1-6, 9-14 and 64 above, and further in view of Yim (U.S. 5,869,395).

The combined teachings of DeSilva, Fiordalice and Huang substantially teach all aspects of the invention but fails to disclose wherein the recess comprises a contact hole situated below a trench, wherein said semiconductor substrate has a lower substrate and terminates at an opposite end thereof at said trench, and wherein said trench extends from said opposite end of said contact hole to a top surface of said dielectric material and parallel to the plane of the lower substrate.

However, Yim (Figs.2A-2K) in a related method to form an interconnect structure teaches the steps of depositing titanium nitride by a chemical vapor deposition process; using chemical-mechanical polishing to remove portions overlaying a damascene trench formed on a dielectric layer (210); providing a recess comprising a contact hole (260) situated below a trench (240); providing a semiconductor substrate (200) having a lower substrate (202) and terminating at an opposite end thereof at said trench (240), wherein said trench (240) extends from said opposite end of said contact hole (260) to a top surface of said dielectric material (210), and parallel to the plane of the lower substrate (202) (Yim, column 4, line 26 – column 7, line 31).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of DeSilva, Fiordalice and Huang with Yim to enable forming the interconnect structure of the combination of DeSilva, Fiordalice and Huang according to

the teachings of Yim because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of forming the disclosed interconnect structure the combination of DeSilva, Fiordalice and Huang and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

6. Claims 65 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeSilva ('736) in view of Huang ('216).

DeSilva (Figs.1-5) teaches a method of forming an interconnect structure including the steps of forming a recess (106, 112) within a dielectric material (102) situated on a substrate (100), the recess (106, 112) extending below a top surface of the dielectric material (102); forming a diffusion barrier layer (116) substantially conformally on the top surface of the dielectric material (102) and over an interior surface of the recess (106, 112); forming an electrically conductive layer (118) on the barrier layer (116) over the top surface of the dielectric material (102) and substantially within the recess (106, 112) such that voids (120, 122) are present within the recess; forming an energy absorbing layer (124) on the electrically conductive layer (118), the energy absorbing layer (124); and utilizing a furnace to apply energy to the energy absorbing layer (124) sufficient to cause the electrically conductive layer (118) to fill the voids (120, 122) within the recess (120, 122) (DeSilva, column 2, line 30 – column 5, line 30).

Furthermore, DeSilva teaches wherein the barrier layer is made of titanium (DeSilva, column 2, lines 54 – 63), the conductive material is made of aluminum (Desilva, column 2, lines 66 – 67) and wherein the energy absorbing layer is made of titanium nitride (DeSilva, column 3, lines 5 – 10).

DeSilva fails to disclose wherein said substrate is a semiconductor substrate; forming a seed layer on the diffusion barrier layer over the top surface of the dielectric material and within the recess, the diffusion barrier layer comprising a material having a melting point greater than or equal to that of a material comprising the seed layer, wherein the material comprising the seed layer is made of aluminum, titanium nitride, titanium, titanium aluminide or comprises tungsten; and removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

However, Huang (Figs.1-8) teaches a method to form an interconnect structure including the steps of forming a recess (13) within a dielectric material (3, 11) situated on a semiconductor substrate (1), the recess (13) extending below a top surface of the dielectric material (3, 11); forming a diffusion barrier layer (9) on the top surface of the dielectric material (3, 11) and over an interior surface of the recess (13), wherein said barrier layer (9) is made of titanium; forming a seed layer (21) on the diffusion barrier layer (9) over the top surface of the dielectric material (3, 11) and within the recess (13), wherein the material comprising the seed layer (21) is made of tungsten, tantalum, or any other refractory metal; forming an electrically conductive layer (17) made of on the seed layer (21) over the top surface of the dielectric material (3, 11) and within the

recess (13); and removing portions of the electrically conductive layer (17) that are situated above the top surface of the dielectric material (3, 11) (Huang, column 4, line 42 – column 5, line 31).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of DeSilva and Huang to enable forming a seed layer in DeSilva according to the teachings of Huang for the further advantage of acting as a nucleation layer (Huang, column 5, lines 8 – 13).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of DeSilva and Huang to enable providing a semiconductor substrate in DeSilva according to the teachings of Huang because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of providing the disclosed substrate in DeSilva and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Also, it would have been within the scope of one of ordinary skill in the art to combine the teachings of DeSilva and Huang to enable removing overlying layers above the dielectric layer of DeSilva according to the teachings of Huang because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of removing overlying layers above said dielectric layer in DeSilva and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Response to Arguments

7. Applicant's arguments with respect to claims 1-6, 9-15 and 64-66 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JULIO J. MALDONADO whose telephone number is

(571)272-1864. The examiner can normally be reached on Mon-Fri, 8:00 A.M.-4:00 P.M..

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/George Fourson/
Primary Examiner, Art Unit 2823

JM
02/15/2008